It is claimed:

1. In a tunable receiver, the improvement comprising:

a filter circuit having a frequency response determined by a value of at least one passive circuit element of a predetermined type in the filter circuit;

a plurality of circuit elements of the predetermined type;

a plurality of switches, each associated with a respective circuit element for switching the respective circuit element into the filter circuit to vary the frequency response of the filter circuit;

a digital interface responsive to digital input signals to control the plurality of switches;

the plurality of circuit elements of the predetermined type, the plurality of switches and the digital interface being incorporated in a single integrated circuit.

2. The digitally tunable filter of claim 1 wherein the digital interface may couple any of the plurality of circuit elements individually, in parallel, or in series with each other into the filter circuit.

3. The digitally tunable filter of claim 2 wherein the values of the plurality of circuit elements are in a binary progression.

4. The digitally tunable filter of claim 3 wherein the circuit elements are capacitances.

5. The digitally tunable filter of claim 1 wherein the digital interface includes conversion circuitry responsive to

the digital input signals to convert the digital input signals to switch control signals.

6. The digitally tunable filter of claim 1 wherein the digital interface includes conversion circuitry responsive to the digital input signals to convert the digital input signals to switch control signals in accordance with a predetermined calibration of the digitally tunable filter.

7. The digitally tunable filter of claim 1 wherein the filter circuit is comprised of at least one resonator.

8. The digitally tunable filter of claim 7 wherein the resonator is comprised of an inductor - capacitance network.

9. The digitally tunable filter of claim 8 wherein the circuit elements are capacitances.

10. The digitally tunable filter of claim 9 wherein the values of the plurality of circuit elements are in a binary progression.

11. The digitally tunable filter of claim 8 wherein the digitally tunable filter circuit, including one or more inductors, is incorporated in the single integrated circuit.

12. The digitally tunable filter of claim 8 wherein one or more of the inductors are printed inductors on a printed circuit board.

13. The digitally tunable filter of claim 12 wherein the printed circuit board is a land grid array (LGA).

14. The digitally tunable filter of claim 8 wherein one or more of the inductors are surface mount inductors, and wherein the rest of the digitally tunable filter circuit is incorporated in the single integrated circuit.

15. The digitally tunable filter of claim 8 wherein one or more of the inductors are printed inductors on a printed circuit board and one or more of the inductors are surface mount inductors attached to said printed circuit board, and the rest of the digitally tunable filter circuits are incorporated in the single integrated circuit.

16. The digitally tunable filter of claim 15 wherein the printed circuit board is a land grid array (LGA).

17. A digitally tunable filter comprising:

a filter circuit having an inductance - capacitance network with a frequency response determined by a value of at least one capacitive element in the filter circuit;

a plurality of capacitive elements;

a plurality of switches, each associated with a respective capacitive element for switching the respective capacitive element into the filter circuit to vary the frequency response of the filter circuit;

a digital interface responsive to digital input signals to control the plurality of switches;

the filter circuit, the plurality of capacitive elements of the predetermined type, the plurality of switches and the digital interface being incorporated in a single integrated circuit.

18. The digitally tunable filter of claim 17 wherein the digital interface may couple any of the plurality of capacitive elements individually, in parallel, or in series with each other into the filter circuit.

19. The digitally tunable filter of claim 18 wherein the values of the plurality of capacitive elements are in a binary progression.

20. The digitally tunable filter of claim 17 wherein the digital interface includes conversion circuitry responsive to the digital input signals to convert the digital input signals to switch control signals.

21. The digitally tunable filter of claim 17 wherein the digital interface includes conversion circuitry responsive to the digital input signals to convert the digital input signals to switch control signals in accordance with a predetermined calibration of the digitally tunable filter.

22. The digitally tunable filter of claim 17 wherein the inductance comprises one or more printed inductors on a printed circuit board.

23. The digitally tunable filter of claim 17 wherein the inductance comprises one or more printed inductors on a printed circuit board and one or more surface mount inductors attached to said printed circuit board.

24. The digitally tunable filter of claim 23 wherein the printed circuit board is a land grid array (LGA).

25. A method of calibrating a digitally tunable filter used in a receiver, the method comprising:

adjusting a plurality of digital control codes associated with said digitally tunable filter;

measuring frequency responses of said digitally tunable filter for the various digital control codes;

characterizing the frequency response of said digitally tunable filter by means of a second set of digital codes; and

storing said second set of codes in a memory.

26. The method of calibrating a digitally tunable filter of claim 25, wherein said frequency responses are comprised of pass bands which pass frequencies associated with desired signals and rejection bands which attenuate frequencies associated with undesired signals.

27. The method of calibrating a digitally tunable filter of claim 26, wherein said rejection bands attenuate frequencies associated with the image signals of said desired signals.

28. The method of calibrating a digitally tunable filter of claim 26, wherein said digitally tunable filter comprises one or more digitally tunable filter resonators.

29. The method of calibrating a digitally tunable filter of claim 28, wherein said digitally tunable filter resonators comprise one or more digitally tunable filter LC networks.

30. The method of calibrating a digitally tunable filter of claim 29, wherein said digitally tunable filter LC networks are implemented on a monolithic integrated circuit.

31. The method of calibrating a digitally tunable filter of claim 29, wherein said digitally tunable filter LC networks comprise networks of fixed value inductors and digitally controlled capacitors.

32. The method of calibrating a digitally tunable filter of claim 31, wherein said networks of fixed value inductors and digitally controlled capacitors are implemented on a monolithic integrated circuit.

33. The method of calibrating a digitally tunable filter of claim 31, wherein said networks of fixed value inductors and digitally controlled capacitors comprise digitally controlled capacitors implemented on a monolithic integrated circuit and inductors external to said monolithic integrated circuit.

34. The method of calibrating a digitally tunable filter of claim 25, wherein said second set of codes are stored in a memory on an integrated circuit wherein said digitally tunable filter is located.

35. The method of claim 34 wherein each of the second set of codes are accessed by a respective one of the various digital control codes.

36. For use in a digitally tunable circuit, the improvement comprising:

an integrated circuit having:

a plurality of capacitor banks, each capacitor bank having a plurality of capacitors having capacitances in a binary progression;

a plurality of switches coupled to each capacitor bank, each plurality of switches being controllable to switch one or more than one of the capacitors in the respective capacitor bank in parallel into another circuit; and,

a control circuit coupled to receive control information and to control the plurality of switches in response thereto.

37. The improvement of claim 36 wherein the switches are FET switches.

38. The improvement of claim 36 wherein the control comprises a shift register coupled to serially receive and store a switch control word, and to control each switch by a respective bit of the control word.

39. The improvement of claim 36 wherein the control comprises a controller and memory.

40. The improvement of claim 39 wherein the controller is coupled to receive a switch control word and to control each switch responsive to the switch control word, the memory being coupled to the controller to store a switch control word received by the controller.

41. The improvement of claim 40 wherein the control is coupled to a serially receive a switch control word.

42. The improvement of claim 39 wherein the controller is coupled to receive calibration information and to store the calibration information in the memory, the controller also being coupled to receive any of a plurality of predetermined control words, each associated with a respective set of

capacitance values to be switched into another circuit, and to use the calibration information stored in memory to control the switches to obtain the capacitance values associated with each predetermined control word received.

43. The improvement of claim 42 wherein the control is coupled to a serially receive a switch control word.